DESIGN OF A NOVEL ONE TRANSISTOR-DRAM BASED ON BULK SILICON SUBSTRATE

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ABSTRACT

In this work, we propose a novel device based on bulk silicon substrate and use it as a dynamic random access memory (DRAM) with TCAD simulation. The operation principle of this device is similar to that of Z²-FET which was demonstrated previously in SOI substrate. In our device, LDD doping and gate control are combined to build up the carrier injection barriers which enable feedback mechanism. The designed device shows similar sharp switch and gate-controlled hysteresis in its output characteristics. It is further demonstrated for DRAM application without need of extra capacitor. The DRAM operation shows high speed and reasonably long retention time.

Keywords— one-transistor dynamic random access memory; feedback mechanism; Z²-FET; bulk substrate;

INTRODUCTION

Z²-FET (zero impact ionization and zero subthreshold swing FET), which is essentially a gate-controlled PIN diode based on silicon-on-insulator (SOI) substrate, is a novel device operating with feedback mechanism between carrier flow and injection barriers [1]. Due to its gate-controlled hysteresis and sharp switching characteristics, it becomes very attractive in many applications, such as logic switch, high performance DRAM and ESD protection [2-4]. The conventional Z²-FET device has the advantages of compact, single front gate footprint, undoped channel, and no impact ionization or bipolar action [5]. Besides, the conventional Z²-FET device also finds applications in flash memory, co-integration in flexible substrate and ion-sensitive sensor [6, 7]. Though the SOI substrate is widely used to build integrated circuits (ICs) with low power, high frequency and radiation hardness, bulk silicon substrate is still dominant in the high performance ICs due to its low cost.

Thus, in this work, we design a novel device based on bulk silicon substrate, which uses similar feedback mechanism as the Z²-FET. The device combines lightly-doped drain (LDD) and the front gate to form the potential barriers and has symmetrical structure as the Z²-FET. It shows similar gate-controlled hysteresis in output characteristics and used as one-transistor DRAM (1T-DRAM) showing excellent performances.

DEVICE STRUCTURE AND OPERATION PRINCIPLE

Figure 1 (a) shows the structure of the designed device. It has very similar structure as conventional p-type MOSFET, except for the opposite source and drain doping type at the same doping concentration of 1020 cm⁻³. The channel is n-type doped with concentration of 10¹⁸ cm⁻³. P-type LDD regions with doping concentration around 10¹⁹ cm⁻³ are formed by ion implantation self-aligned to the front gate. The distance between channel and source/drain regions is defined by the spacer in a self-aligned way. The gate length and spacer length (LG and Lspr) are both 50 nm. From source to drain, a P⁺-P-N⁺ structure is formed, which is similar to a thyristor.
Synopsys Sentaurus is used to simulate the device. Conventional physic models are used in the simulation. The potential profile of the device from source to drain is extracted and shown in Fig. 1(b). Hole and electron injection barriers similar to that found in Z2-FET are observed. The electron injection barrier is formed by the PLDD region next to the source, and marginally affected by the gate voltage. However, the hole barrier is formed in the channel and dramatically modulated by the front gate voltage. Due to the feedback between carrier flows and their potential barriers, a sharp switch behavior is observed in the output characteristics, see Fig. 1(c). The ID-VD curves of this device also show large hysteresis window with the turn-on voltage controlled by the front gate voltage (VG). This is attributed to the hole potential barriers modulated by the VG.

APPLICATION AS 1T-DRAM

The designed device is further used as DRAM which needs no extra capacitor. It is truly a 1T-DRAM which is more compact than conventional 1T1C-DRAM. The charge is directly stored in the front gate capacitor (C_G) formed by the gate oxide to represent the logic state of the device and read out through feedback mechanism. Figure 2 shows the waveforms of the DRAM operation. In order to write logic “0”, a negative V_G pulse down to 0V is used to discharge the gate capacitor. Without extra charge in the gate capacitor, the read of the device by a positive V_D pulse failed to turn on the device. Thus, the device stays in OFF state during read “0” process.

On the contrary, during write logic “1” state, the V_G reduces from 1V down to 0V, meanwhile V_D rise up from 0V to 1.2V. Since the hole injection barrier is largely reduced by V_G = 0V, V_D =1.2V can easily turn on the device, as the I_D curve indicates in Fig. 2. Large amount of electrons and holes are injected into the channel during ON state. Electron charges are stored in the gate capacitor as the V_G goes back to 1V. These charges can cause transient electron current during the read process when V_D pulses up to 1.2V. The transient electron current flows into the drain and is amplified by the internal feedback loop, which eventually turns on the device, as shown in Fig. 2. This process is similar to that in Z²-FET [5]. Unlike conventional 1T1C-DRAM which needs large amount of charge to reliably drive external buffer amplifier, our novel DRAM stores only small amount of charge to trigger the internal feedback loop and thus has very fast operation speed down to 1ns. A preliminary study is also performed on the retention time of this device. Figure 3(a) shows that after writing “O”, the read of the device correctly outputs low current. However, after 1 sec, the read of the device outputs high current, which indicates the failure of stored “O”. This is due to that, during holding “0”, electron-hole pairs are regenerated in the depleted channel by thermal generation and tunneling. In contrast, the stored charge never loses since V_G = 1V is applied during hold process.

Thus, logic “1” is a steady state and needs no refresh. Figure 3(b) shows that reads of logic “1” correctly output high current after 1 sec and 10 secs.

CONCLUSION

A novel device is demonstrated with similar operation principle as the Z²-FET. The device is based on bulk-Si substrate instead of SOI. By combining LDD doping and gate control, a potential profile with electron and hole injection barriers are formed in the channel, which leads to gate controlled hysteresis. This property is further used for DRAM operation. Without need of extra capacitor, the novel DRAM shows compact form and high operation speed down to 1ns. A preliminary study is also performed on the retention time of both logic “0” and “1” states. With high operation speed, high integration density, and based on widely-used bulk-Si substrate, the proposed device is expected to attract lots of interests.
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REFERENCES