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A Novel 8T TFET-MOSFET Hybrid SRAM Cell For Ultra-Low Power And Computing In-memory Applications

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ABSTRACT

In this work, a novel 8T Tunnel FET (TFET)-MOSFET hybrid SRAM design with awareness of the impacts of large gate-drain capacitance in TFET is proposed and simulated. The proposed design utilizes MOSFET and TFET as upper and down transistor respectively in the read path, which can avoid the voltage coupling in conventional cascade TFET structure. Compared with conventional 6T CMOS SRAM, it achieves significant reduction in static and operation power, as well as improved static noise margin (SNM), leading to the lowest read power-delay-product (PDP). Moreover, its application for multiply-and-accumulate (MAC) operations in analog computing in-memory (CIM) is also demonstrated with high energy efficiency showing its great potential for energy-efficient AIoT applications.

INTRODUCTION

- **Unique Electrical Characteristics of TFETs**
  - **Unidirectional conduction**
  - **Forward p-i-n current (I_{PIN})**
    - These two may lead to functional errors or increased power consumption, and have been considered in previous studies.
  - **Large gate-drain capacitance (C_{GD})**
    - This will cause delay issue and has rarely been considered.
- **A new 8T TFET-MOSFET hybrid SRAM cell design with consideration of C_{GD} for better PDP has been proposed and application in CIM is demonstrated.**

DESIGN OF 8T HYBRID SRAM CELL

- **The design employs a cross-coupled inverter structure.**
- **Write path: MOSFETs as dual-ended access transistors.**
- **Read path: a series connection of a MOSFET and a TFET, with the TFET's drain connected to RBL through a MOSFET and its source connected to ground.**
  - Pulse on WR can be coupled to RBL through C_{GD}
  - Smaller C_{GD} in MOS → smaller signal spikes in V_{RBL} → smaller read delay

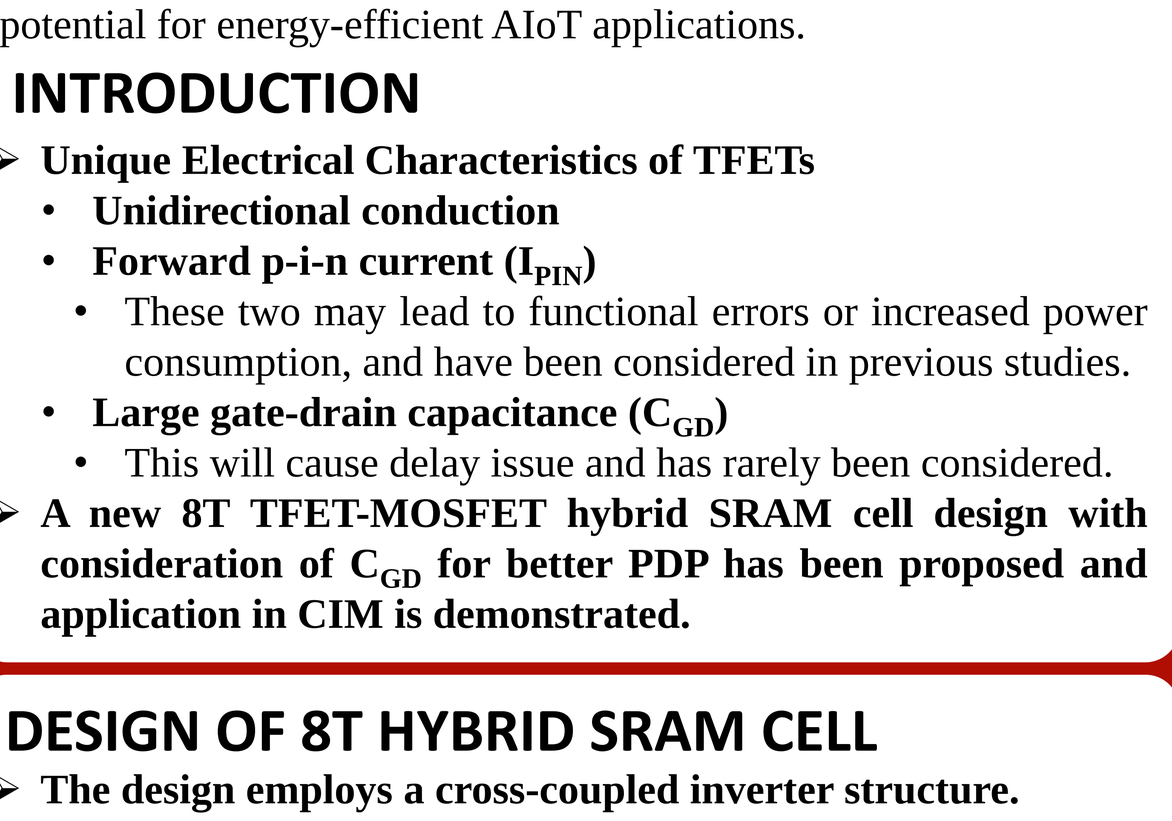

Fig 1: (a) Proposed 8T design & Operations (b) Hold (c) Write (d) Read.

RESULTS & DISCUSSION

- **Comparison for different SRAM topologies:**
- **Delay**
  - Read delay is reduced by 97.92% compared with conventional 8T due to voltage coupling from node x to gate of Tn3, read delay is larger than 6T CMOS SRAM.
  - Write delay is the same as conventional 8T but higher than 6T CMOS SRAM.
- **PDP**
  - Read PDP is 75.68% lower than the conventional 8T and 5 orders of magnitude lower than the 6T CMOS SRAM.
  - Write PDP is similar to the conventional 8T and 1 order of magnitude lower than the 6T CMOS SRAM.

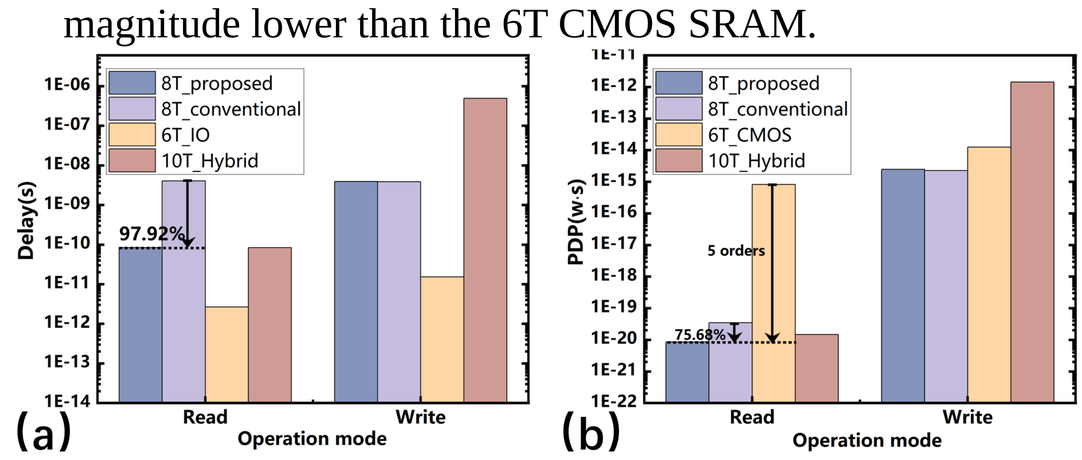

Fig 2： benchmark of different SRAM topologies.

- **CIM Application:**
  - When multiple rows of WRs are activated, each bitcell performs an input-weight product (IWP) operation, and the result will multiply by column on RBL.
  - The MAC results exhibit good linearity.

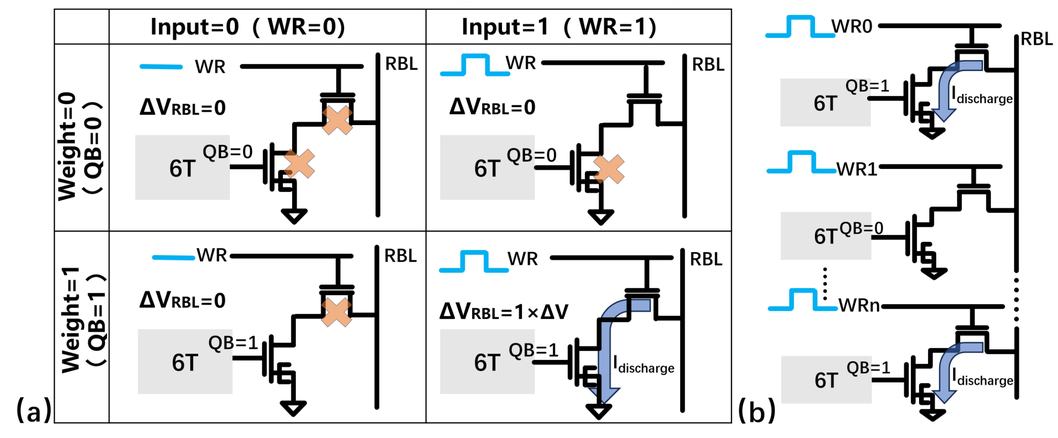

Fig 3： (a) IWP operation; (b) MAC operation of multi-rows.

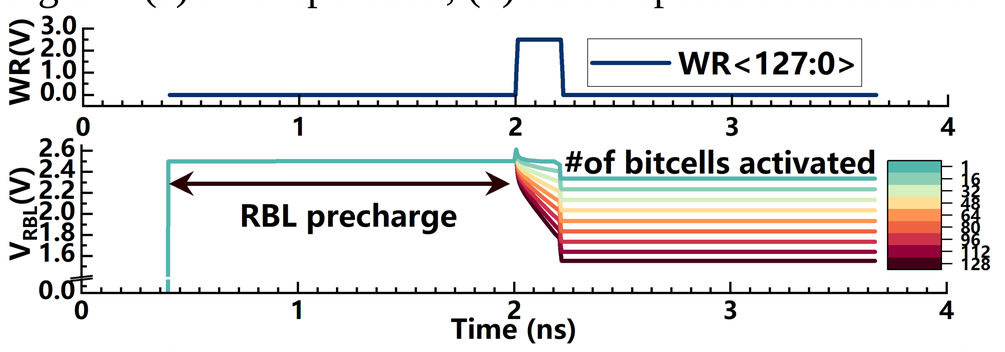

Fig 4： Simulation waveforms of MAC operations in one column.

SUMMARY

This work presents a novel 8T TFET-MOSFET hybrid SRAM showing considerably power and PDP reduction compared with 6T CMOS SRAM and other reported TFET SRAM designs respectively. Additionally, MAC operation can be realized utilizing the proposed SRAM with higher energy efficiency of one order of magnitude than that of 6T CMOS SRAM array. The result shows the great potential of TFET SRAM in ultra-low power application.