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上海华力 HLMC

THE NOVEL STRATEGY OF PATTERN GATE HIGH LOADING CONTROLING IN ILD0 CMP PROCESS

Shuxiang Wang*, Yurong Qu, Zhenxing Zhu, Mingfei Yu, Jingxu Fang, Yu Zhang
Advanced Module Research & Development Dept., Shanghai Huali Integrated Circuit Corp., Shanghai 201314, China.

Introduction

As the semiconductor device size reduced to 28nm or smaller, the HKMG technology was gradually introduced into the chip manufacturing process to improve the response speed and reliability of devices. In the gate-last scheme, after MG-CMP, the gate height in the short channel region is lower than that in the long channel region. The large pattern gate high loading leads to electrical anomalies eventually. In this paper, three strategies based on ILD0-CMP were explored for controlling gate height loading.

Result & Discussion

■ The scheme of ILD0-CMP & MG-CMP

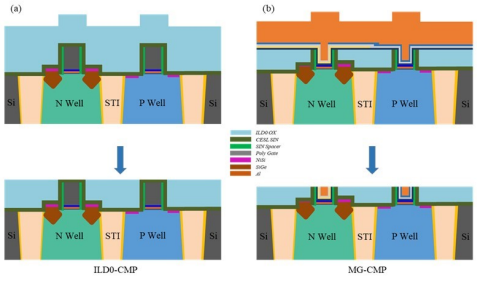

Figure 1: The scheme of (a)ILD0-CMP and (b)MG-CMP

✓Gate height control ✓Residue defect free

■ The process of ILD0-CMP with AMAT tool

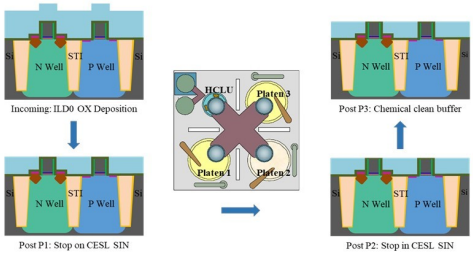

Figure 2: The configuration of ILD0-CMP polish module

✓P1 by EDP + P2 by time

■ The new strategies of RMG loop

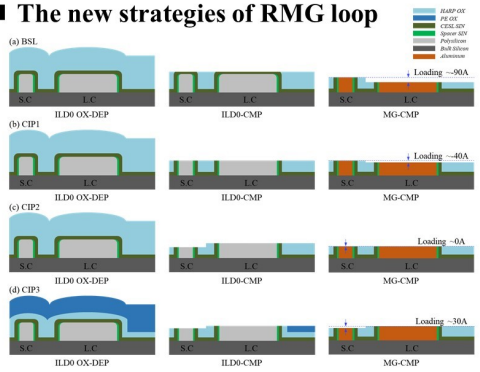

Figure 3: The (a)BSL and (b)(c)(d)CIP scheme of RMG loop

✓ P2 Stop layer, P2 slurry, ILD OX film

■ Weak-point pattern gate height result

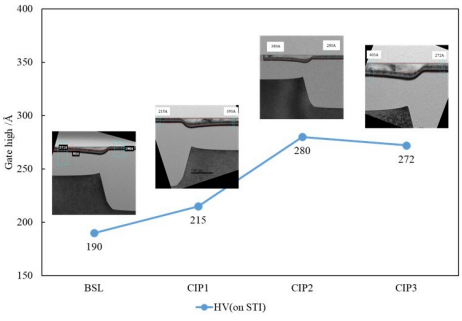

Figure 4: The TEM result of weak-point pattern gate height

✓ The weak-point pattern G.H. is improved

Conclusion

The alteration of process stop layer, P2 slurry and ILD OX film in ILD0-CMP exhibited a positive effect on the controlling of gate height loading post MG-CMP.

The TEM result show gate height loading improved 57-97% and the gate height in weak device region increased 13%-47% post MG-CMP process, the RMG loop process window is enlarged.

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