Process Window Optimization for Gate Etch Process of 2D NAND

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Abstract

Two dimensional (2D) NAND has been used in applications such as industrial control systems and automotive electronics. Manufacturers working on further scale traditional planar NAND face significant challenges in processing high aspect ratio (HAR) structures. This paper focuses on the gate etch process of 2D NAND, presenting findings from a systematic investigation conducted using SEMulator3D®, a 3D predictive modeling software. The analysis reveals that the formation mechanisms of two primary defects during the gate etch, active area (AA) pitting and fence defects, are intricately linked to the control of oxide-nitride-oxide (ONO) spacer height in the control gate (CG), ONO and floating gate (FG) etch processes. Furthermore, the defect process window is explored, highlighting the critical importance of both ONO/poly selectivity and poly etch amount control. Ensuring a proper balance is essential for managing spacer height effectively. During actual gate etch process tuning, pattern loading emerges as the most challenging issue, including the trade-offs between pitting, fencing and profile loading across different patterns. Effective strategies have been implemented to optimize the process window. The findings of this investigation not only reveal the key lesson learned for the control of AA pitting and fence defects, but also provide guidance for appropriate gate etch recipe design and process window optimization.

Keywords—2D NAND; Pitting defect; Fence defect; Process window optimization; Pattern loading; SEMulator3D®

Introduction

Two-dimensional (2D) NAND, a typical non-volatile memory technology, has been widely used for data storage[1] and has become an integral part of consumer electronics, automotive electronics, and data centers. Although three-dimensional (3D) NAND technology has been upstaging in recent years, there continues to be demand for 2D NAND in applications such as industrial control systems, automotive electronics, and security and protection systems, driven by the high reliability required in these sectors. However, as the technology node advances, maintaining reliability and performance becomes increasingly difficult. The dimensions of 2D NAND are approaching physical limits, posing significant obstacles to further miniaturization[2], particularly in the gate etch process, which is constrained by a narrow process window and multiple process limitations and trade-offs.

In this paper, we have systematically investigated the gate etch process, employing both simulation using the SEMulator3D® virtual fabrication platform and experimental procedures on actual silicon wafers. The 3D predictive modeling software analysis has unveiled that the formation mechanisms of two typical defects during the gate etch, active area (AA) pitting and fence defects. are intimately connected to the control of oxide-nitride-oxide (ONO) spacer height in the control gate (CG), ONO and the floating gate (FG) processing steps. Additionally, we have explored the defect process window based on the ONO/poly selectivity and poly etch amount at the ONO steps. This exploration underscored the importance of both selectivity and etch amount control, emphasizing the necessity of maintaining an appropriate balance for the precise control of spacer height. During actual gate etch process tuning, pattern loading was revealed as the most challenging issue, including the trade-offs between pitting, fencing and profile loading across different patterns. Effective strategies have been implemented to optimize the process window.

Experiment description

In our experiment, the gate etch process was simulated using SEMulator3D® virtual fabrication software. We established the gate etch short loop flow in the software, and subsequently calibrated the model using actual silicon wafer data. The formation mechanism of two main defects, AA pitting defect and oxide fence defect, were simulated. To further explore the gate etch process window, we varied ONO/Poly selectivity and poly etch amount at ONO etch steps to check the pitting and fence defect performance. Based on the understanding on the gate etch process, several technical strategies were investigated to improve the etch loading performance on the actual silicon wafer.

Result and Analysis

Gate etch is one of the most challenging applications in 2D NAND fabrication, involving the patterning of the CG, ONO, and FG with hard mask (HM). The pattern structure and film stacks of gate etch are illustrated in Figure 1, where SiO2 and SiN films serve as the HM. The FG has been patterned into lines during the shallow trench isolation (STI) etch process, followed by STI oxide filling, STI chemical mechanical polishing (CMP) and recess to the median height of FG. ONO films are then deposited along the FG, creating a topography of ups and downs, followed by the deposition of the CG film resulting different the CG film thicknesses between the AA and the STI areas. During the CG etch process, CG must be cleared up and stopped on the top oxide layer in both AA and STI areas. At the ONO etch steps, the top ONO films on FG are first opened, then the ONO spacer at the FG shoulders and FG itself are etched simultaneously with a certain selectivity. The remaining FG is cleaned up by FG etch steps, which also pulls down the oxide spacer and forms STI recess.

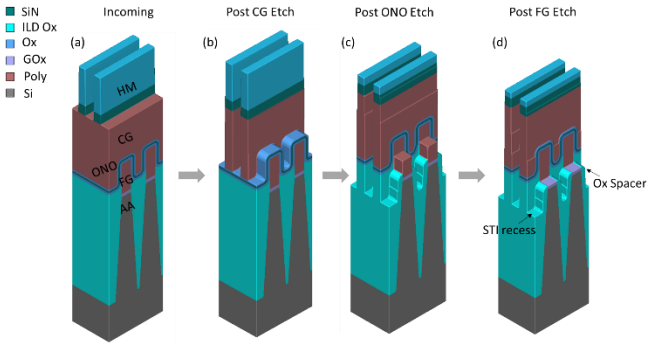

Figure 1. Schematics for the incoming film stack and by-step structure evolution of 2D NAND gate etch. (a) Post HM open. (b) Post CG etch; (c) Post ONO etch; (d) Post FG etch.

With such high aspect ratio (HAR) structure (AR >10) and multiple materials to be etched, the gate etch process becomes very challenging. The unique Poly-ONO-Poly structure and varying pattern features further narrow the gate etch process window, introducing numerous process trade-offs. AA pitting and oxide fence defects are two typical defects in the gate etch process. Ideally, the ONO spacer height should be precisely controlled by adjusting the etch amount and selectivity during ONO and FG etch steps to ensure that the top of the oxide spacer is level with the top of the gate oxide, as shown in Figure 2b and prevent the formation of AA pitting and spacer fence defects. However, it is difficult in practical to simultaneously control the vertical FG profile and selectivity among oxide, nitride, and poly films across different patterns. Simulation results indicate that when the ONO to poly selectivity is low and/or the etch amount is large, the oxide spacer height is pushed below the AA top. This exposes the AA sidewall to plasma, damaging the silicon during the FG etch process and resulting in AA pitting defects, as shown in Figure 2d. On the other hand, when the ONO to poly selectivity is high and/or the etch amount is small, the remaining oxide spacer is too high to be fully consumed during the FG etch steps, leading to the final oxide fence defect, as shown in Figure 2f.

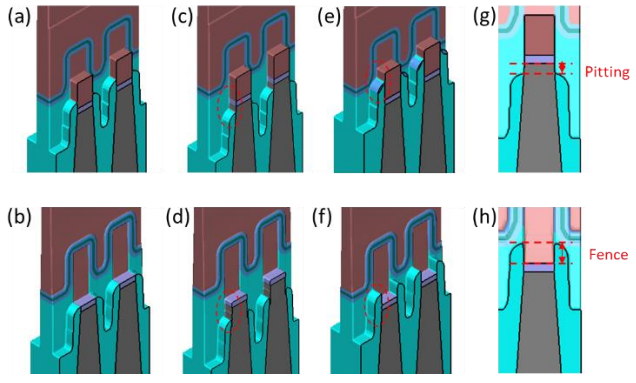

Figure 2. Pitting and fence defect. (a)-(b) Ideal etch structures post ONO etch and final etch, respectively. (c)-(d) Etch structures post ONO etch and final etch of pitting defect, respectively. (e)-(f) Etch structures post ONO etch and final etch of fence defect, respectively. (g)-(h) The schematics of AA pitting and fence measurement.

Virtual DOEs are conducted using SEMulator3D® to explore the process window to break the AA pitting defect and spacer fence defect trade-off. The defects performance of DOE splits based on ONO/poly selectivity (1.0-2.5) and poly etch amount (25-50 nm) at ONO steps are investigated. It is revealed that there is a process window with no pitting and fence defects with proper ONO/poly selectivity and poly etch amount control. However, the green area is quite small, indicating that the process window is very narrow (Figure 3).

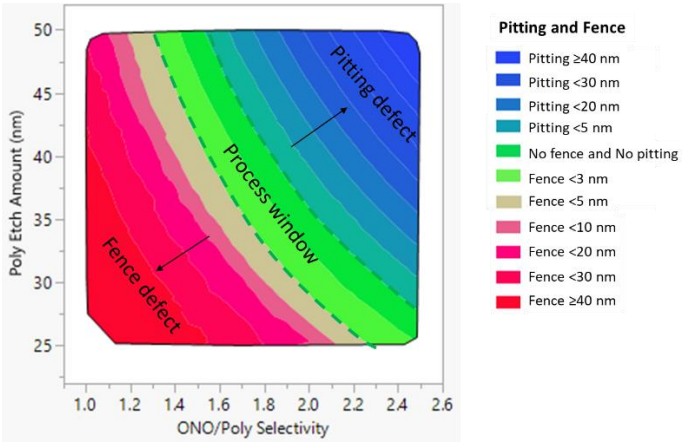

Figure 3. Contour map of ONO/Poly selectivity and poly etch amount at ONO etch step impact on final pitting and fence defect window of gate etch.

On actual silicon wafer, there are different patterns with varied line and space dimensions, resulting etch loading effect due to different AR and etch volume. Although fine-tuning the etch process can yield a vertical gate profile without pitting and fence defects for a specific pattern, replicating this optimal performance across multiple patterns is very challenging. This difficulty stems from the dependence of etch process on the volume of the material to be etched. As illustrated in Figure 4, pattern A has a larger space dimension and requires etching of substantial volume of polysilicon. This results in a local depletion of etch radicals in this area, thereby reducing the etch rate and potentially leading to the formation of polysilicon residues and spacer fence defects. On the other hand, pattern B requires lesser volume of polysilicon removal compared to pattern A. The abundance of etch radicals facilitates a higher etch rate, which can result in bowing of the FG profiles and the emergence of AA pitting defects.

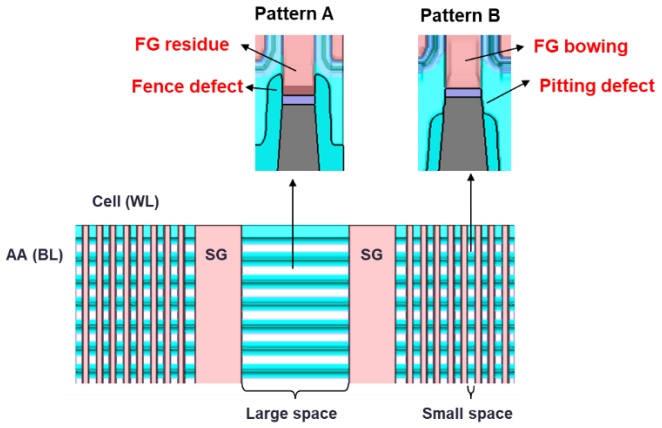

Figure 4. Pattern loading shown between patterns with different space. Pattern A with large space shows fence defect and FG residue issue; Pattern B with small space shows pitting defect and FG bowing issue.

The baseline gate etch for 2D NAND is conducted in Lam

Research Kiyo series etcher. Based on test results on silicon wafers, tuning pattern B to achieve a vertical FG profile without defects results in bowing FG profile and AA pitting defects in pattern A. On the other hand, tuning pattern A to a vertical profile without defects leads to FG residue and fence defects. To mitigate the loading induced FG profile difference and pitting-fence defects trade-offs, several technical solutions have been implemented. After implementing bias pulsing at the FG and ONO etch steps, both AA pitting and fence defects were mitigated (CIP1 in Fig. 5). By tuning the CG etch step to a higher selectivity regime, fence defects were eliminated with only slight pitting defects remaining (CIP2 in Fig. 5). Further gas tuning at the CG and FG etch steps finally resulted vertical gate profiles, breaking the process trade-offs (CIP3 in Fig, 5).

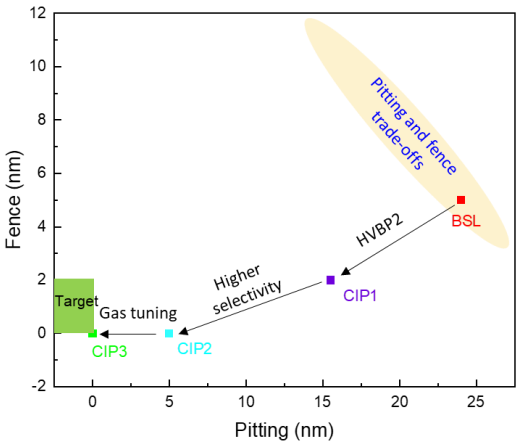

Figure 5. Process window optimization to break pitting and fence trade-offs.

Conclusion

In conclusion, the 2D NAND gate etch process was simulated using the SEMulator3D® platform. The formation mechanism of AA pitting and fence defects was found to be related to the control of ONO spacer height during the CG, ONO, and FG etch processes. A virtual DOEs were conducted to explore the process window, identifying a defect-free regime through fine control of ONO/poly selectivity and poly etch amount. Tests on silicon wafers demonstrated that poly profile and defect trade-offs across different patterns can be resolved using bias pulsing and recipe tuning with more advanced features. Our study not only elucidates the gate etch defect formation mechanism and mitigation strategies but also highlights the time and cost-saving benefits of SEMulator3D for process window checks and optimization.

Reference

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