Zero-defect Solutions for Automotive Semiconductor Devices Manufacturing

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ABSTRACT

Automotive semiconductor devices need to cope with harsh conditions and complex tasks in the vehicle environment, so there are stringent qualification and verification standards and complex testing and monitoring requirements for device manufacturing. The goal of zero-defect is key to the efficient, reliable and high-volume production of automotive semiconductor devices. This review describes how Lam Research Corp. is providing solutions to achieve zero-defect performance in all areas (wafer frontside, edge/bevel, and backside) of the entire wafer. Frontside defects can be reduced by innovative honeycomb gas injector and Corvus® design in Kiyo® series etcher. Black Si defects at wafer bevel/edge can be inhibited by bottom shadow ring (BSR) on Syndion®, or bevel deposition or etching approaches on Coronus®. For arcing defects caused by tungsten (W) residual in edge area, DOMOER design in ALTUS® reduces W residual after CMP. Wafer backside deposition by VECTOR® DT not only compensates for wafer profile, reducing crack or peeling defects caused by wafer wrapping, but also acts as a barrier layer to suppress the doing effect from highly doped substrate to frontside epitaxial layers of power and CMOS image sensor (CIS) devices.

Keywords — Automotive semiconductors; Zero defect; Bevel defect, backside deposition.

INTRODUCTION

In recent years, governments around the world have vigorously developed hybrid and pure electric vehicles (EV) to achieve energy sustainability and address climate change caused by greenhouse gases (GHG).[1-4] With the changes in the automotive industry, the trend towards highly electrification and intelligent vehicles has driven the growth in demand for chips in automotive. Automotive electronic systems are the key enablers, which can be divided into traditional core engine control, safety, body & convenience, car audio, as well as car electrification, advanced driver-assistance system (ADAS), networking, positioning and connectivity under digitalization and electrification.[5] In the past, a traditional car was equipped with an average of about 500 to 600 chips of distinct types. Today, high-end new energy vehicles even require more than 2,000 chips, highlighting the core position of chips in the automotive industry.[6]

Compared with consumer electronics or general industrial products, the design, manufacturing, and verification process of automotive semiconductor devices are extremely complex and need to pass a series of strict certifications of international standards, such as AEC-Q100, ISO/TC 176, ISO26262 and so on.[7-11] Automotive electronics need to be exposed to harsh environments and need to be able to adapt to temperatures ranging from -40 to 150°C. Their lifespan needs to be more than 15 years, and they have higher requirements for low defective rates (ppm level) and device consistency, stability and repeatability.[12] Therefore, quality control is extremely important to manufacture automotive electronic devices, enhance product competitiveness, and establish industry barriers efficiently and stably. Any systematical problems in the manufacturing process, such as defects, may threaten the life and health of vehicle users in the future, and ultimately cause immeasurable economic and reputational losses to the automotive company and semiconductor device manufacturer. Therefore, continuous improvement and zero-defect solutions have become the goals that automotive semiconductor manufacturers are constantly striving for.[13-17] Worth noted that, it often takes three years or more for automotive semiconductor devices to be developed and verified. Therefore, mature tools with large install base will accelerate automotive development cycle and lower the final cost.

In this paper, we will demonstrate how Lam's mature and stable tools are providing zero-defect solutions in all areas of wafer. Part I, we will talk about how we reduce wafer frontside fall-on defects, which come from polymer accumulation on chamber parts. In Si power trench fabrication, we reduce wafer frontside defects by 95% with innovative honeycomb gas injector and Corvus® design in Kiyo® series etcher. Part II, we will discuss how to prevent defects from wafer bevel/edge. For black Si defects

generated during the silicon deep trench etching, we can use BSR in Syndion® etcher to protect the Si substrate from being etched or implement bevel deposition in Coronus® tools. For arcing defects caused by W residual in edge area, DOMOER design in ALTUS® optimizes bevel W film during W deposition and reduces W residual after CMP with arcing free. In Part III, we will introduce our solutions on backside defectivity control. Wafer backside deposition by VECTOR® DT not only compensates for wafer profile, reducing crack or peeling defects caused by wafer wrapping, but also acts as a barrier layer to suppress the doing effect from highly doped substrate to frontside epitaxial layers of power and CMOS image sensor (CIS) devices. We also introduce dripping reduction solutions (DRS) during Power/CIS wafer thinning processes.

Part I, Wafer Frontside Defect Management

Wafer frontside defect control is very crucial since it will impact wafer yield directly. Frontside defects may come from fall-on defects from upper chamber or sidewall. And fall-off defects are most likely related to polymer accumulation or bombardment effect on upper chamber. Reducing polymer accumulation should draw great attention from automotive device manufacturers.

Deep trench etching is one critical process for low voltage power discrete devices, which has been mass production on Lam Kiyo® tool. Varying with device design and clear ratio, Si deep trench etching process may transit to high power and high flow region. Sufficient byproduct polymers are required during the etch process to meet profile requirements as trench goes deeper and deeper. During its long processing, such byproduct polymers may also accumulate on the gas injector. We found some plasma light-up within gas injector for some deep trench etching and polymers drop on wafer center, resulting in 1~3% yield loss. Our plasma simulations, as shown in Figure 1, indicate honeycomb interface can block the plasma and reduce the byproduct polymer accumulation within the injector by geometry optimization. No center defect is found after >600 RF hours with the honeycomb injector in low voltage Si deep trench (~6µm).

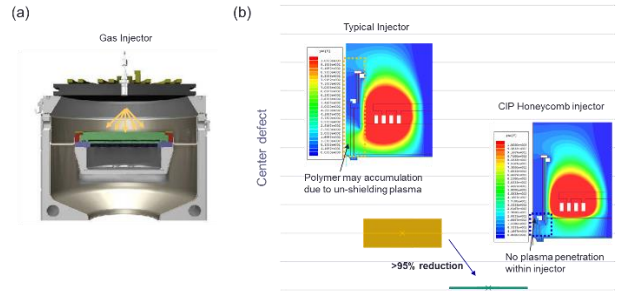

Figure 1: (a) Gases are delivered from chamber top plate in standard ICP chambers. (b) Plasma simulation indicates that typical gas injector may suffer plasma attack and polymer accumulation within injector, while honeycomb injector blocks plasma penetration and demonstrates 95% reduction in center defects during silicon deep trench etching.

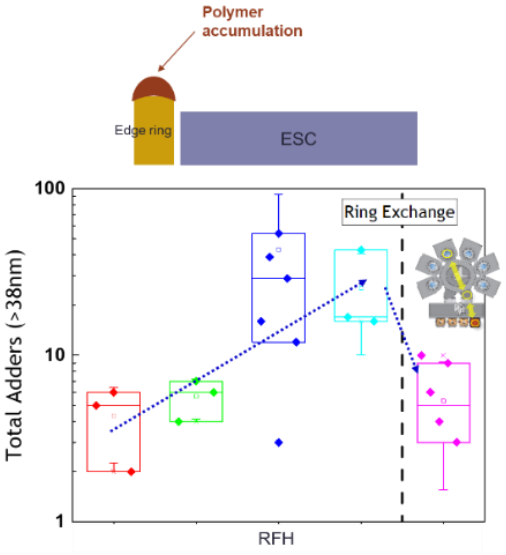

Figure 2: Corvus™ R can enable a particle reset when edge ring accumulation is a mechanism for particles.

Beside gas injector, polymer may also accumulate around edge ring and backflow onto wafer frontside. The particle or defect performance may get worse as RF hour (RFH) increases. To clean and reset polymer accumulation at chamber edge ring, some productivity solutions like Lam waferless auto clean (WAC) have been used to maintain good chamber condition. To further improve particle performance and chamber utility, Lam's Corvus® R is designed to replace edge ring regularly without breaking vacuum. We can reset the particle performance and keep it within a tight spec after ring exchange (shown in Figure 2).

Part II, Wafer Edge/Bevel Defect Management

The wafer edge or bevel region is also very important for yield improvement when power devices move from 8-in to 12-in. Even though no device is expected there, the edge or bevel defects may lead to edge yield loss. Among the edge or bevel defects, black Si defect is very common during power/ICS device Si deep trench etching.

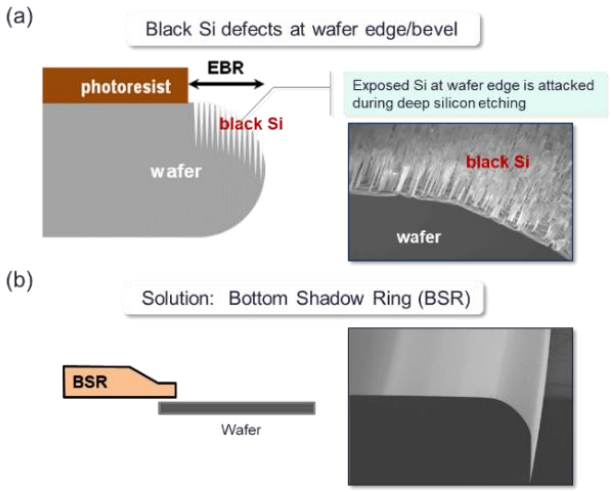

Figure 3: (a) Black Si defects are observed at wafer edge or bevel post deep Si etch in power discrete or CIS wafer fabrication. (b) Bottom shadow ring (BSR) protects wafer edge without black silicon defects on Syndion® series tools.

Generally, during device fabrication, photoresist accumulates at the edge of the silicon wafer, resulting in poor pattern formation in the edge area. Edge bead removal is required post lithography. However, when conducting deep silicon etching (~µm) on CIS and power discrete wafers, the EBR area is easily damaged due to the lack of mask protection, forming black Si defects as shown in Figure 3(a). Lam provides BSR on Syndion® series tools to protect wafer bevel/edge, with the optional BSR ring size (1 to 2mm overlap between BSR and wafer edge) to compensate with different EBR among products. As shown in Figure 3(b), black Si defect is eliminated.

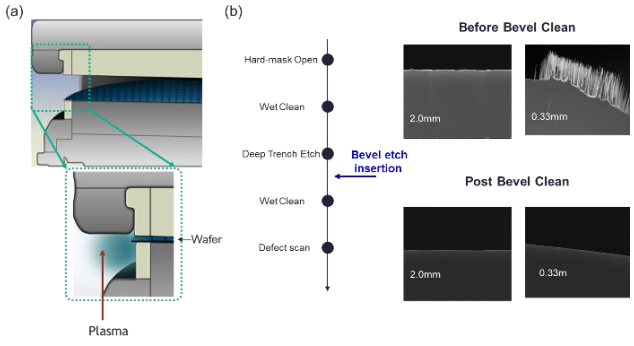

Figure 4: (a) Coronus® tool schematic to realize wafer bevel management and (b) bevel etch insertion post deep trench etch remove Si needle defects from wafer edge and bevel zones.

For those shallow or medium Si trenches etched in typical ICP chambers (like Kiyo®) without BSR ring, wafer bevel management using Coronus® can be inserted in the integration flow to remove black Si defects as well. In Figure 4(a), it shows the schematic of Coronus® chamber. Only part of wafer edge and bevel region are exposed to plasma, and the plasma is confined by insulator rings. The upper and lower plasma exclusion zones (UPEZ and LPEZ) are defined by the configurable ring size, up to 4mm from the Apex. The left panel of Figure 4(b) shows the process flow of Si deep trench loop. After the hard-mask opening, the mask layers at bevel region are removed at EBR region. Therefore, the substrate is etched together with Si trenches within wafer. Severe black Si defects could be found at bevel region. After bevel etch insertion post deep trench etching, it finally demonstrates a defect-free and flat surface and thus reduces wafer bevel defect sources.

Besides the etching approach, oxide or carbon films can be deposited in bevel area only using Coronus® chamber. Inserted post hard-mask open, the bevel oxide or carbon (in µm thickness) will act as a new mask and prevent wafer substrate from being etched. The bevel oxide or carbon layers can be removed by wet cleaning or striping after deep trench etching. Figure 5shows the defect-free performance delivered by this approach.

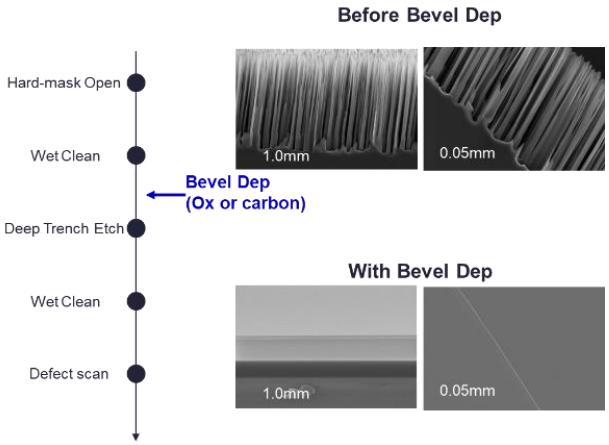

Figure 5: Bevel deposition (oxide or carbon) effectively protects wafer substrate during high aspect ratio silicon etching (in super junction devices).

Metal residuals at bevel region may introduce ball defects due to wafer arcing. As schematically shown in Figure 6(a), W deposition may show thickness difference between wafer center and bevel region. W residuals may be found at the bevel region after CMP process, which becomes the arcing sources in the subsequent ILD deposition or via etching process step under CCP plasma. DOMOER design uses backside gas to control W deposition profile at wafer edge and bevel regions. In Figure 6(b), we can tell that the W profile with DoMOER shows steep profile at wafer bevel, thus less W residual. With this new design, we can ultimately achieve ball defect free performance.

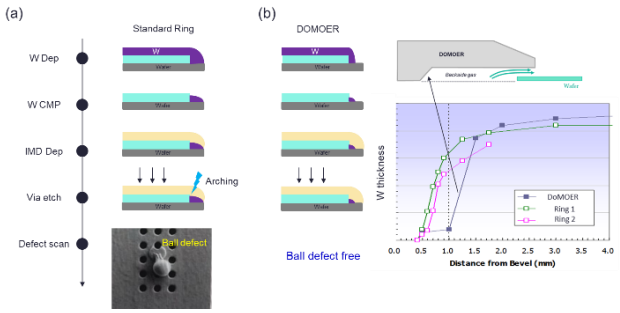

Figure 6: (a) Ball defects are observed post oxide via etch due to arcing. (b) DOMOER design optimizes bevel W film during W CVD and reduces W residual post CMP.

Part III, Wafer Backside Defect Management

Wafer backside is usually regarded as less impact on device performance or final yield. However, in power/CIS wafers, high-stress films during device fabrication may lead to wafer warpage, and cause integration issues including lithography de-focus, ESC clamping failure, wafer sliding, arcing, bonding failure, etc. Wafer backside defects, like cracking, may originate from film stress. Surface streak defects post wafer backside thinning are also one of the main concerns for electrical performance in power devices.

For wafer backside stress management, Lam provides direct backside deposition solution in VECTOR® DT to be seamlessly inserted into wafer processing flows for wafer bow management. Figure 7(a) illustrates the enabling hardware for direct backside deposition, in which taco, umbrella or saddle shape wafer profile could be compensated by proper backside deposited films. Wafer is lifted by carrier rings in PECVD chamber and reaction gases flow from bottom showerhead-pedestal while CCP plasma is sustained in between wafer backside and pedestal to deposit high stress SiO2/SiN films (from -1200 MPa to +600 MPa) per integration needs. Figure 7(c) shows the stress measurements after HDP poly fill ess in power devices, wafer bow can reach -500 µm without backside bow compensation. With VECTOR® DT backside film deposition, wafer bow can be maintained as low as 100 µm, which meets the lithography bow requirements (≤±200 µm).

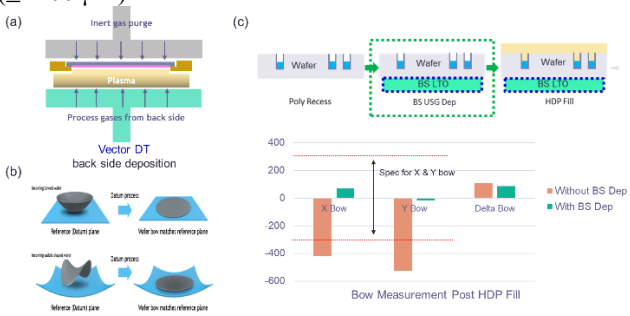

Figure 7: (a) VECTOR® DT chamber structure to realize backside deposition. (b) bow management is crucial for wafer processing, like lithography focus and wafer chucking. (c) HDP filling shows large wafer bowing, which is compensated by BS deposition.

Besides stress management to make wafer profile as flat as possible, backside deposition films by VECTOR® DT can also act as barrier layers. Power and CIS devices require heavily doped silicon substrates, which may cause cross contamination during the following high temperature (>1000˚C) epitaxial growth of frontside device layers, and result in device resistance non-uniform issue. Such an auto-doping effect can be eliminated by pre-deposition of a backside sealing layer. Lam's VECTOR® DT provides an approach for backside sealing layer deposition without the need of wafer flipping and bevel etching. Figure 8 shows that a larger than 5 times reduction in resistance non-uniformity can be achieved by 2.5kÅ or 3 kÅ backside oxide deposition.

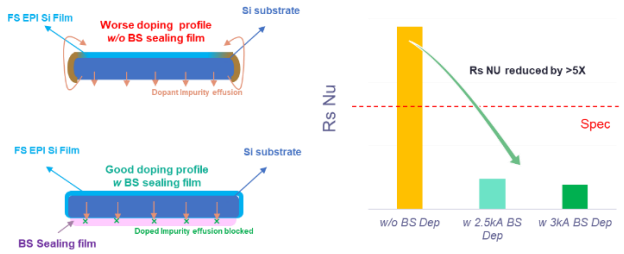

Figure 8: Backside sealing also blocks the dopant effect from highly doped substrate to frontside epi layers.

Wafer thinning in CIS and power devices by wet etch is a very important fabrication step for better device performance. For example, ultrathin wafer in power devices shows the benefits of lower on resistance, package height reduction and heat dissipation improvement. During wafer backside thinning, chemical dripping could generate visible surface streak defects. The stains can lead to poor adhesion between silicon metal films and can impact the electrical parameter performances of power devices. Dripping Reduction Solution (DRS) design can deliver stable dripping prevention by optimizing nozzle geometry. The chemical suction happens exactly when the chemical is switched off. The adhesive forces will be enhanced between dispenser tube and chemicals, so that the inner surface aging effect can be compensated by robust liquid meniscus formed. As shown in Figure 9(b), we have successfully eliminated the average dripping defects after using DRS nozzle.

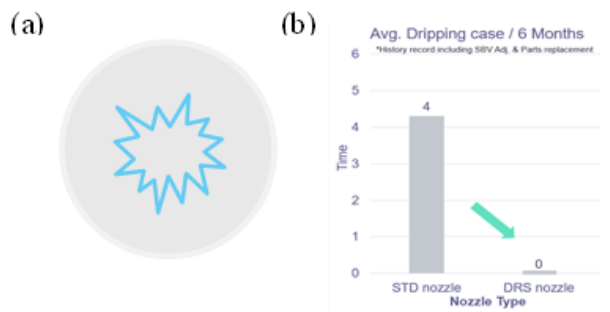

Figure 9: (a) non-optimized suck back control in power/CIS wafer thinning can induce defects and local non-uniformity. (b) optimized geometry of dripping reduction solution (DRS) nozzle minimizes the switch-off effect and eliminates the average dripping defects.

Summary

In this paper, we introduced zero-defect control solutions for automotive semiconductors (including power, CIS and other devices) from Lam Research. Lam provides mature and stable solutions to lower the defect risk in all wafer areas (frontside, edge/bevel, and backside). For wafer frontside, we can use honeycomb gas injectors to reduce potential fall-on defects from the gas injectors, and Corvus™ R to reset particle performance without vacuum break. For wafer edge and bevel regions, both of BSR in Syndion® and bevel deposition/etch solutions with Coronus® can help to eliminate black Si defects during Si deep trench etching. Our innovative DoMOER design in W CVD could reduce W residual at wafer edges, then deliver arcing free in the following ILD deposition and via etch steps. As for the wafer backside, VECTOR® DT can help to compensate wafer bowing, and block the dopant effect between high-doped Si substrate and epi layer on power and CIS wafers. DRS nozzles can eliminate dripping defects during wafer backside thinning. All these hardware optimal designs can help to accelerate automotive semiconductor devices manufacturing and qualification, together with Lam's process and productivity maintenance methods.

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